AMENDMENTS TO THE CLAIMS[INS1]

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (Previously Presented) Phase locked loop charge pump comprising:

a drain node; and

at least a cascode transistor for limiting the variation of the voltage of said drain node,

wherein an intermediate switch transistor is placed between the drain node and the cascode transistor.

2. (Currently Amended) The charge pump of claim 1, said charge pump comprising a first node, a second node, a branch connecting the first node with the second node, said branch comprising a first cascode transistor and a second cascode transistor, a first switch transistor is coupled across from ~~placed in parallel to~~ the first cascode transistor, and a second switch transistor ~~placed in parallel~~ coupled across from ~~to~~ the second cascode transistor, further comprising an intermediate switch transistor between the drain node and a cascode transistor, coupled across from ~~in parallel to~~ one of the first switch transistor and the second switch transistor.

3. (Currently Amended) The charge pump of claim 2, further comprising two intermediate switch transistors, a first intermediate transistor between the first node and the first cascode transistor, said first intermediate transistor being coupled across from ~~in parallel to~~ the first switch transistor, the second intermediate switch transistor being between the second node

and the second cascode transistor, said second intermediate transistor being coupled across from ~~in parallel to~~ the second switch transistor.

4. (Currently Amended) The charge pump of claim 3, wherein the first switch transistor coupled across from ~~in parallel to~~ the first cascode transistor and/or the second switch transistor ~~in parallel to~~ coupled across from the second cascode transistor is connected to a further cascode transistor coupled across from ~~in parallel to~~ the first and/or second cascode transistor.

5. (Currently Amended) The charge pump of claim 4, wherein the first switch transistor ~~in parallel to~~coupled across from the first cascode transistor and a further cascode transistor form a dummy branch ~~in parallel to~~coupled across from the first cascode transistor and the first intermediate transistor, said dummy branch having connections so as to be controlled by the complement signal of the signal controlling the first intermediate transistor and/or the second switch transistor ~~in parallel to~~coupled across from the second cascode transistor and a further cascode transistor form a dummy branch ~~in parallel to~~coupled across from the second cascode transistor and the second intermediate transistor, said dummy branch having connections so as to be controlled by the complement signal of the signal controlling the second intermediate switch transistor.

6. (Previously Presented) An electronic circuit comprising a charge pump according to claim 1.

7. (Previously Presented) An integrated circuit comprising a charge pump according to claim 1.

8. (Previously Presented) A phase locked loop charge pump comprising:
a drain node;

a first cascode transistor to limit the variation of the voltage of said drain node;

a first intermediate switch transistor positioned between said drain node and said first cascode transistor; and

a dummy branch with a second cascode transistor connected to a second intermediate switch transistor,

wherein said second intermediate switch transistor is positioned between said first node and said second cascode transistor.